REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Official Action of December 18, 2006 (hereinafter, "Office Action"). In response, Applicants have canceled Claims 4-9 and 14-20, and have amended the remaining claims to clarify the recitations thereof in light of the cited references. In addition, Applicants have added new dependent Claims 36-41. Applicants submit that the recitations of these claims are fully supported by the present specification as originally filed, and as such, no new matter has been added. Accordingly, Applicants respectfully submit that pending Claims 1-3, 10-13, 21, and 36-41 are patentable over the cited art for at least the reasons discussed below.

The Section 101 Rejections

Claims 1-3 stand rejected under 35 USC §101 as lacking patentable utility for failing to provide concrete, tangible, and useful results. *See* Office Action, Page 2. The MPEP further describes the utility requirement as follows:

> The claimed invention as a whole must be useful and accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." *State Street*, 149 F.3d at 1373-74, 47 USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (*citations omitted*).

MPEP, §2106 (*emphasis added*).

In response, Applicants respectfully submit that the claims recite results which are useful, tangible, and concrete, in full compliance with U.S. case law and the USPTO's Guidelines for Examination of Computer Related Inventions. For example, independent Claim 1 as amended recites:

> 1. A method for testing a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, the method comprising:
>
> extending y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to the nm memory cell arrays in a test data write step; and

> comparing the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data, and outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step.

Accordingly, the present subject matter is directed to **testing memory cell arrays of a semiconductor memory device**, which Applicants submit meets the requirements for a practical application. For example, some problems presented in testing memory cell arrays are discussed (in detail) in Applicants' background:

> A conventional semiconductor memory device tester may use a parallel bit test (PBT) technique to test more than one semiconductor memory device at the same time. The PBT technique does not receive or output data through all of the data I/O pads of the semiconductor memory devices, but only through a predetermined number of data I/O pads, thereby allowing for simultaneous testing of a larger number of semiconductor memory devices.
>
> For example, if a tester has 32 data I/O terminals and a semiconductor memory device operating at a single data rate (SDR) receives or outputs 16-bit data, only two semiconductor memory devices can be tested simultaneously. However, using the PBT technique, 4 or 8 semiconductor memory devices can be tested at the same time, as data can be received or output through 8 or 4 data I/O pads, respectively.

Specification, Page 1, line 22 to Page 2, line 2. Accordingly, Applicants submit that the claims provide a "real world" use in selecting data for output to test semiconductor memory devices. Moreover, as the claims recite "memory cell arrays" and "data I/O pads", Applicants submit that the claims recite subject matter that represents more than just an idea or concept.

Applicants further submit that the claims recite a tangible and concrete result. For example, the recitations of "extending y-bit data received through y data I/O pads to (nm×x)-bit data ", "comparing the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data", and "outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads" are, at least, as tangible as determining a price of a share of stock, which was held to meet these requirements in *State Street Bank & Trust Co. v. Signature Financial Group Inc.*, 149 F. 3d 1368, 1374, 47 USPQ2d 1596, 1601-02 (Fed. Cir. 1998). Furthermore, the claims

fully comply with the New Guidelines set out by the USPTO on October 26, 2005[1].

Accordingly, Applicants respectfully maintain that Claims 1-3 recite statutory subject matter in compliance with the utility requirement of 35 USC §101. As such, Applicants respectfully request withdrawal of the rejections under §101 for at least the above reasons.

The Section 112 Rejections

Claim 1 also stands rejected under 35 USC §112, second paragraph, as being incomplete for omitting essential steps, as required by MPEP §2172.01. In particular, the Office Action asserts that Claim 1 recites a method for testing a memory cell array, but the steps for performing such testing are missing. *See* Office Action, Page 2.

However, Applicants note that the cited portion of the MPEP provides:

> A claim which omits matter disclosed to be essential to the invention as described in the specification or in other statements of record may be rejected under **35 U.S.C. 112**, first paragraph, as not enabling. *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). See also **MPEP § 2164.08(c)**. Such essential matter may include missing elements, steps or necessary structural cooperative relationships of elements described by the applicant(s) as *necessary* to practice the invention.
>
> In addition, a claim which fails to interrelate essential elements of the invention as defined by applicant(s) in the specification may be rejected under **35 U.S.C. 112**, second paragraph, for failure to point out and distinctly claim the invention. See *In re Venezia*, 530 F.2d 956, 189 USPQ 149 (CCPA 1976); *In re Collier*, 397 F.2d 1003, 158 USPQ 266 (CCPA 1968). >But see *Ex parte Nolden*, 149 USPQ 378, 380 (Bd. Pat. App. 1965) ("[I]t is not essential to a patentable combination that there be interdependency between the elements of the claimed device or that all the elements operate concurrently toward the desired result"); *Ex parte Huber*, 148 USPQ 447, 448-49 (Bd. Pat. App. 1965) (A claim does not necessarily fail to comply with 35 U.S.C. **112**, second paragraph where the various elements do not function simultaneously, are not directly functionally related, do not directly intercooperate, and/or serve independent purposes.).

MPEP §2172.01 (*emphasis added*). As such, Applicants submit that Claim 1 as amended neither omits nor fails to interrelate any matter disclosed to be essential or necessary to

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[1] See http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf

practice the invention in view of the prior art. For example, as noted in the present application:

> For example, in some embodiments of the invention, a memory cell array of a semiconductor memory device which operates as a single data rate internally receives or outputs 32-bit data, the number of selected row selecting signal lines is 2, and the number of selected column selecting signal line is 4. When a test is performed by a conventional parallel bit test method, at least 8 data I/O pads may be required, but when a test is performed by the present invention, only 4 data I/O pads may be required. That is, further embodiments of the present invention may operate such that a read operation may be repeatedly performed until all of the comparison result data has been selectively output by the selecting circuit.
>
> Therefore, circuits and methods according to embodiments of the present invention may allow fewer data I/O pads to be used in parallel bit testing. As a result, a greater number of semiconductor memory devices can simultaneously be tested.

Specification, Page 12, lines 17-28 (*emphasis added*). Accordingly, Applicants submit that the recitations of "extending y-bit data received through y data I/O pads to (nm×x)-bit data ", "comparing the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data", and "outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads" provided in Claim 1 as amended particularly point out and distinctly claim the essential steps for performing the testing of a memory cell array to reduce the number of data I/O pads to be used in parallel bit testing so that a greater number of semiconductor memory devices can be simultaneously tested.

Thus, Applicants respectfully request withdrawal of the rejections under §112 for at least the above reasons.

The Section 102 Rejections

Claim 1 stands rejected under 35 U.S.C. §102(a) as anticipated by Applicant Admitted Prior Art (U.S. Patent Application Publication No. 2004/0252549; hereinafter "AAPA"). Claim 1 as amended, for example, recites:

> 1. A method for testing a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, the method comprising:
>
> extending y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to the nm memory cell arrays in a test data write step; and
>
> comparing the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data, and outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step. (*Emphasis added*).

Applicants respectfully submit that the AAPA fails to disclose or suggest at least the recitations of Claim 1 as amended highlighted above. For example, the Office Action relies on the AAPA as disclosing selecting first comparison data corresponding to one of the plurality of memory regions for output via an input/output pad, and selecting second comparison data corresponding to another of the plurality of memory regions for output via the input/output pad. *See* Office Action, Page 3. However, the cited portion of the AAPA provides:

> The 4 memory cell regions (5) to (8) each respectively receive 4-bit data ODI1~4, ODI5~8, ODI9~12, and ODI13~16 in a write operation mode, and each respectively output 4-bit data ODO1~4, ODO5~8, ODO9~12, and ODO13~16 in a read operation mode. The column redundant memory cell array **12** is used to replace a column selecting signal line with a redundant column selecting signal line when a defect occurs in the memory cells connected to the column selecting signal lines ECSL1, ECSL2, OCSL1, and OCSL2 of the memory cell array **10**. The row redundant memory cell array **14** is used to replace a row select line with a redundant row select line when a defect occurs in the memory cells connected to the row select lines WL1 and WL2 of the memory cell array **10**.

AAPA, Paragraph 0011, lines 15-28. Accordingly, the cited portion of the AAPA describes four memory cell regions (5) to (8) that receive and output 4-bit data in write and read operation modes, respectively, and a column redundant memory cell array 12 and a row redundant memory cell array 14. As such, nowhere does the cited portion of the AAPA disclose or suggest the recitations of Claim 1 highlighted above.

In addition, the AAPA further describes:

> The comparator **16** compares, by 4 bits, test data EDO1~4, EDO5~8, EDO9~12, EDO13~16, ODO1~4, ODO5~8, ODO9~12, and ODO13~16 output from the memory cell regions (1) to (8), respectively, to generate 8-bit comparison result data MA1 to MA8 in a parallel bit test operation mode. The 8-bit comparison result data MA1 to MA8 is output from the memory device through the data I/O pads DQ1, DQ3, DQ5, DQ7, DQ9, DQ11, DQ13, and DQ15. That is, the comparison result data obtained from comparing the 4-bit data output from the memory cell regions (1) to (8) are output from the memory device through 8 data I/O pads DQ1, DQ3, DQ5, DQ7, DQ9, DQ11, DQ13, and DQ15.

AAPA, Paragraph 0011, lines 28-40 (*emphasis added*). In other words, the AAPA describes generating comparison data MA1 to MA8 corresponding to the memory regions (1) to (8), and outputting the comparison data from each of the eight memory regions (1) to (8) to eight different data I/O pads. More particularly, Figure 2 of the AAPA illustrates that data signals EDO1-EDO4 from memory region (1) are compared to generate result data MA1, which is output to pad DQ1. Likewise, data signals EDO5-EDO8 from memory region (2) are compared to generate result data MA2, which is output to pad DQ3. *See* AAPA, Fig. 2. Accordingly, the AAPA discloses that 8 data signals from 8 different memory regions are output to 8 *different* input/output pads.

In contrast, Claim 1 as amended recites "outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads". Nowhere does the AAPA disclose or suggest selecting *nm*-bit comparison data by *y* bits for output to *y* data I/O pads. Rather, as noted above, the 8-bit comparison data MA1 to MA8 from the different memory regions are output to 8 different I/O pads. In other words, the number I/O pads required to output the comparison data in the AAPA corresponds to the number of bits of the comparison data, as each bit is output to a different I/O pad. Accordingly, Applicants respectfully submit that the AAPA fails to disclose or suggest at least the recitations of Claim 1 highlighted above. Thus, Applicants submit that Claim 1 as amended is patentable for at least the above reasons. Claims 10 and 11 as amended include similar method and device recitations, and as such, are patentable for at least similar reasons. Also, dependent Claims 2-3 and 12-13, and 39-41 are patentable at least per the patentability of Claims 1, 10, and 11 from which they depend.

The Section 103 Rejections

Independent Claim 21 stands rejected under 35 U.S.C. §103(a) as obvious over the AAPA in view of U.S. Patent No. 7,013,413 to Kim et al. (hereinafter "Kim"). Claim 21 as amended recites:

> 21. (Currently Amended) A semiconductor memory device, comprising:
>
> nm memory cell arrays configured to respectively output x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1;
>
> a test data write circuit configured to extend y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to the nm memory cell arrays wherein nm is integer time as greater as y; and
>
> a test data read circuit configured to compare the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data, group and output the nm-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to a control signal, and output y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads. (*Emphasis added*).

Applicants respectfully submit that the combination of the AAPA and Kim fails to disclose or suggest at least the recitations of Claim 21 as amended highlighted above. For example, the Office Action concedes that the AAPA fails to disclose or suggest a selecting circuit configured to select first comparison data corresponding to one memory region and second comparison data corresponding to another memory region for output via the same input/output pad, but argues that Kim provides these recitations. *See* Office Action, Page 6.

> Applicants respectfully disagree. As provided by the cited portion of Kim:
>
> Referring to **FIG. 4**, in a memory device according to an embodiment of the present invention, the read data comparing part **500** comprises a number of comparators **501-508** for receiving 8 bits data RD<0:7> read from the core cell region **100** according to a control signal (S_DATEST) when it is a DA mode test, compressing upper 4-bit data RD<0:3> and a lower 4-bit data RD<4:7> and generating a 1-bit data error<i>, 0<i<7, having information indicating whether a failure exists, multiplexers **509-512** for selecting the 8-bit data RD<0:7> read from the core cell region **100** when it is a normal mode or

> error <0:7> generated by the comparators **501-508** when it is a DA mode test according to the control signal (S_DATEST).

Kim, Col. 4, lines 55-67 (*emphasis added*). Accordingly, Kim discloses a circuit including comparators **501** to **508** that compare write data WD and read data RD to generate error signals error<0> to error<7>, respectively. As further illustrated in Figure 4 of Kim, the multiplexer **509** selects between the read data RD<0:7> (in normal mode) and the error data error<0:7>(in test mode) for output to the data pad DQB0 based on the control signal S_DATEST. *See* Kim, Fig. 4. More particularly, Kim describes:

> The multiplexer **509** selects the error <0:7> compressed by the comparators **501-508** during a DA mode test according to the control signal (S-DATEST). That is, the data New RD<0:7> selected via the multiplexer **509** can be either error<0:7> or the read data RD<0:7>. The selected parallel data is forwarded to the shift register **301** where the data is transformed into an even-bit part and an odd-bit part and further converted into serial data via the multiplexer and driver **401** of the interface part **400** and outputted via a corresponding output pad DQB0.

Kim, Col. 6, lines 4-13. As such, the error signals are forwarded in parallel through a multiplexer **509**, a shift register **301**, and a multiplexer & driver **401** that serially outputs the data through a data output pad DQB0 in response to test clock signal TestClkR during a test mode. *See also* Kim, Fig. 4

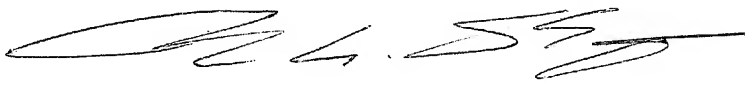
However, nowhere does the cited portion of Kim disclose or suggest a test write circuit configured to extend y-bit data received through y data I/O pads to ($nm \times x$)-bit data in a test data write operation, nor a test read circuit configured to compare the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data, group and output the nm-bit comparison result data into y groups, and output y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads in a test read operation. Accordingly, Applicants submit that the circuit of Kim fails to disclose the "test data write circuit" and the "test data read circuit" as recited in Claim 21 as amended. Moreover, as noted above with reference to Claim 1, the AAPA also fails to disclose or suggest these recitations.

Accordingly, Applicants submit that the combination of Kim and the AAPA does not disclose or suggest at least the recitations of Claim 21 highlighted above. Thus, Applicants submit that Claim 21 as amended is patentable the for at least the above reasons. Also, dependent Claims 36-38 are patentable at least per the patentability of Claim 21 from which they depend.

Conclusion

Accordingly, based on the remarks provided above, Applicants respectfully submit that all of the pending claims are now in condition for allowance. Thus, Applicants respectfully request withdrawal of the outstanding rejections, allowance of the pending claims, and passing the application to issue. Applicants encourage the Examiner to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,



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